UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,208	12/20/2001	Jang Geun Oh	LT-0007	6134

34610 7590 03/01/2005

FLESHNER & KIM, LLP
P.O. BOX 221200
CHANTILLY, VA 20153

EXAMINER
HENRY, MATTHEW ALLAN

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/022,208	OH, JANG GEUN	
	Examiner	Art Unit	
	Matthew A. Henry	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 10-21 and 23-25* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because:

Figures 6 and 8 are partially completed using handwriting. Please complete the drawings in type and to exclude mistakes to enhance their clarity.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the second clock described in Claims 23-25 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 23-25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The claims mention "generating a second clock for the CPU and the controlling device" that is not mentioned in the description of the invention. In the background of the invention, mention of a second clock is made, however the signal is not directed to the CPU and controlling device.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh in view of Weidner.

Concerning Claim 1, Yeh teaches:

A bus clock controlling method (Column 3, Lines 28-32) in a computer (Figure 1, Item 10; Column 2, Line 62), comprising:

setting a throttle rate of a clock to a predetermined initial value (Figure 2, Item 100; Column 4, Lines 49-53), the clock being used for a data bus (Figure 1, Item 32; Column 3, Lines 2-5) connected between a CPU (Figure 1, Item 20; Column 2, Lines 66-67) and a controlling device (Figure 1, Item 30; Column 2, Line 67);

detecting a user's pressing of a button (Figure 2, Item 102; Column 4, Lines 56-58) if a present power source is at least one battery (Column 1, Lines 16-18); and

adjusting the set throttle rate according to the user's button press (Figure 2; Item 104; Column 4, Lines 59-61).

Yeh teaches of adjusting the bus clock frequency based upon a user's button press instead of the remaining battery capacity.

Weidner teaches:

detecting a remaining battery capacity (Column 5, Lines 39-41).

adjusting the set throttle rate according to the detected remaining battery capacity (Column 5, Lines 42-45).

The motivation behind the device disclosed by Weidner is the understanding that when power resources are limited, there is an important goal of maximizing power usage. Weidner states that generating a clock of a lower frequency will conserve power (Column 5, Lines 35-39).

It would have been obvious to a person of ordinary skill in the art to modify Yeh's ability to set a bus clock rate based upon user interaction with the method of varying clock rates automatically based upon the remaining amount of power available to a system as taught by

Weidner. This combination would have resulted in the mutual goal of maximizing the usage of a power supply by varying the bus clock rate.

Concerning Claim 2, Weidner further teaches:

said adjusting step increases the set throttle rate as the detected remaining battery capacity decreases (Column 5, Lines 42-45; a decrease in clock rate is equivalent to an increase in throttle rate).

Concerning Claim 3, Yeh further teaches:

said adjusting step selects one value appropriate to the detected remaining battery capacity among a plurality of throttle rates preset in reverse proportion to different remaining battery capacities (Figure 2, Items 114l and 114h; the range of values detected can be one of only two values, low and high which are further tied to a corresponding and predefined frequency rate).

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh as applied to claim 1 above, and further in view of Young.

Concerning Claim 4, Yeh and Weidner fail to teach of using a bridge controller as a controlling device.

Young teaches:

said controlling device is a bridge controller in a computer (Column 1, Lines 20-23).

Young is similarly motivated in providing a method for "dynamically controlling clock speed on a bus system that does not require human intervention" (Column 2, Lines 41-42). His justification for this is that "supplying a full speed clock at all times is energy efficient" (Column 1, Lines 50-51). PCI systems are widely used in computers and Young demonstrates a "typical PCI system" (Column 1, Lines 17-18) incorporates a bridge circuit. Therefore, it would have been obvious to a person of ordinary skill in the art to use a bridge controller as a controlling device, so that the advantages of combining Yeh and Weidner can be used for a PCI system.

7. Claims 5-7 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh in view of Atkinson.

Concerning Claim 5, Yeh teaches:

A bus clock controlling method (Column 3, Lines 28-32) in a computer (Figure 1, Item 10; Column 2, Line 62), comprising:

setting a throttle rate of a clock to a predetermined initial value (Figure 2, Item 100; Column 4, Lines 49-53), the clock being used for a data bus (Figure 1, Item 32; Column 3, Lines 2-5) connected between a CPU (Figure 1, Item 20; Column 2, Lines 66-67) and a controlling device (Figure 1, Item 30; Column 2, Line 67);

detecting the pressing of a button by a user (Figure 2, Item 102; Column 4, Lines 56-58)

adjusting the set throttle rate in response to the pressing of a button by a user (Figure 2; Item 104; Column 4, Lines 59-61).

Yeh teaches of adjusting the bus clock frequency based upon the pressing of a button by a user rather than the load on the CPU and, though he notes the inverse relationship between bus

clock frequency and power consumption performance, does not teach of adjusting the rate in reverse proportion to the load of the CPU.

Atkinson teaches:

detecting a present load of the CPU (Column 5, Lines 5-7)

adjusting the set throttle rate in reverse proportion to the present CPU load (Column 5, Lines 10-17).

The motivation for the device disclosed by Atkinson lies in the amount of power needed to supply a portable computer (Column 1, Lines 56-61). Atkinson attempts to extend the battery life in a portable computer by adjusting the clock frequency based upon the activity of the system.

Both Yeh and Atkinson offer ways of reducing power consumption based upon adjusting clock frequencies. Incorporation of Atkinson into Yeh would have created a system that accurately optimizes a bus clock according to system activity rather than user interaction. Therefore, it would have been obvious to a person of ordinary skill in the art to combine the bus clock varying system based upon user interactions described by Yeh with the clock adjusting system based upon system activity described by Atkinson to take advantage of its accurate clock optimization technique.

Concerning Claim 6, Yeh further teaches:

said adjusting step is conducted only when a present power source is at least one battery (Column 1, Lines 16-18).

Concerning Claim 7, Yeh further teaches:

The method set forth in claim 5, wherein said adjusting step includes selecting a new throttle rate appropriate to the detected CPU load from a plurality of throttle rates preset in reverse proportion to different CPU loads (Figure 2, Items 114l and 114h; the range of values detected can be one of only two values, low and high which are further tied to a corresponding and predefined frequency rate).

Concerning Claim 17, Yeh teaches:

A bus clock controlling method (Column 3, Lines 28-32) in a portable computer (Figure 1, Item 10; Column 2, Line 64), comprising:

setting a throttle rate of a clock to a predetermined initial value (Figure 2, Item 100; Column 4, Lines 49-53), the clock being used for a data bus (Figure 1, Item 32; Column 3, Lines 2-5) connected between (Column 3, Lines 5-8) a controlling device (Figure 1, Item 30; Column 2, Line 67) and a selected one of a plurality of devices (Figure 1, Item 50; Column 3, Line 1) associated with the portable computer;

detecting (Figure 1, Item 78; Column 4, Lines 41-42) a condition of a prescribed criteria (Figure 2, Item 112; Column 5, Lines 21-23) of the portable computer if a present power source is a battery (Column 1, Lines 16-18); and

adjusting the set throttle rate according to the detected condition (Figure 2, Item 118; Column 6, Lines 1-2), wherein the detected condition is within a range of values for the prescribed criteria (Figure 2, Items 114l and 114h; Column 5, Lines 22-24; the range of values detected can be one of only two values, low and high).

Yeh does not disclose the prescribed criteria being either the condition of a remaining battery or a CPU load.

Atkinson teaches:

Detecting a condition of CPU load (Column 5, Lines 5-7).

The motivation for combining Yeh with Atkinson can be seen above in the Claim 5 rejection.

Concerning Claim 18, Yeh teaches:

the selected device is a peripheral device (Figure 1, Item 60; Column 3, Line 1; the video card is peripheral by being attached yet not integral to the functioning of the CPU), and wherein the predetermined initial value is a smallest throttle rate (Figure 2, Item 100; Column 4, Lines 49-55).

Concerning Claim 19, Yeh further discloses:

said adjusting step selects a rate corresponding to the detected condition among a plurality of prescribed throttle rates that each correspond to mutually exclusive sets of values of the detected condition within the range of values for the prescribed criteria (Figure 2, Items 114l and 114h; Column 5, Lines 22-24; the range of values detected can be one of only two values, low and high).

8. Claims 8, 11, 16 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh in view of Weidner, and further in view of Atkinson.

Concerning Claim 8, Yeh teaches:

A computer (Figure 1, Item 10; Column 2, Line 62), comprising:

a CPU that processes (Figure 1, Item 20; Column 2, Line 66-67);

a first controller (Figure 1, Item 30; Column 2, Line 67) coupled to the CPU via a data bus (Figure 1, Item 32; Column 3, Lines 3-4), and configured to provide a throttled clock (Column 3; Lines 30-32) to the data bus (Column 6, Lines 15-19) according to a throttle rate;

a clock generator (Figure 1, Item 40; Column 3, Line 11); coupled to the CPU (Figure 1, Item 34; Column 3, Line 13) and the first controller (Figure 1, Item 34; Column 3, Line 14), and configured to generate a clock (Column 3, Lines 11-13);

a detector (Figure 1, Item 78; Column 4, Lines 41-42) detecting a variable (Figure 1, Item 75a; Column 4, Lines 25-27), wherein the variable is whether or not a user has pressed a button.

a second controller (Figure 1, Item 70; Column 3, Lines 1-2) coupled to receive the detected variable (Figure 1, Item 75; Column 4, Lines 23-27), configured to determine the throttle rate according to the detected variable (Figure 2, Item 112; Column 5, Lines 22-24), and further configured to output the throttle rate to the first controller.

Yeh teaches a variable that is the user's button press rather than the CPU load or remaining battery capacity. Additionally,

Weidner teaches:

a detector detecting a variable, wherein the variable is a remaining battery capacity (Weidner, Column 5, Lines 39-41).

a second controller coupled to receive the detected variable, configured to determine the throttle rate according to the detected variable and further configured to output the throttle rate to the first controller (Column 5, Lines 39-45).

The motivation for combining Yeh with Weidner can be seen above in the Claim 1 rejection.

Atkinson teaches:

a detector detecting a variable, wherein the variable is a load of the CPU (Column 5, Lines 5-7).

The motivation for combining Yeh with Atkinson can be seen above in the Claim 5 rejection.

Atkinson and Weidner do not teach of considering the variable being a remaining battery capacity *or* a load of the CPU. However, it would have been obvious to a person of ordinary skill in the art, recognizing that both the remaining battery capacity and the CPU load are factors which may be considered as a reason for altering a bus clock frequency to save power, to create a system that can vary the bus clock frequency based upon the CPU load or the remaining battery capacity.

Concerning Claim 11, Weidner further teaches:

the throttle rate increases as a value of the detected variable decreases (Column 5, Lines 42-45; a decrease in clock rate is equivalent to an increase in throttle rate).

Concerning Claim 16, Yeh teaches:

A bus clock controlling method (Column 3, Lines 28-32) in a computer (Figure 1, Item 10; Column 2, Line 62), comprising:

setting a throttle rate of a clock to a predetermined initial value (Figure 2, Item 100; Column 4, Lines 49-53), the clock being used for a data bus (Figure 1, Item 32; Column 3, Lines 2-5) to which both a CPU (Figure 1, Item 20; Column 2, Lines 66-67) and a controlling device (Figure 1, Item 30; Column 2, Line 67) are connected;

detecting the pressing of a button by a user (Figure 1, Item 78; Column 4, Lines 41-42) a remaining battery capacity and a load of the CPU if a present power source is a battery (Column 1, Lines 16-18); and

adjusting the set throttle rate according to the detected remaining battery capacity and the CPU load (Paragraph 110, Lines 1-2).

Yeh does not teach the detection of remaining battery capacity or the CPU load or the adjustment to the throttle rate based upon the remaining battery capacity and the CPU load

Weidner teaches:

detecting a remaining battery capacity (Column 5, Lines 39-41); and

adjusting the set throttle rate according to the detected remaining battery capacity (Column 5, Lines 42-45).

The motivation for combining Weidner and Yeh can be seen in the above claim 1 rejection.

Atkinson teaches:

detecting a load of the CPU (Column 5, Lines 5-7).

adjusting the set throttle rate according to the detected CPU load (Column 5, Lines 10-17).

The motivation for combining Yeh with Atkinson can be seen above in the Claim 5 rejection.

Atkinson and Weidner do not teach of considering the variable being a remaining battery capacity *and* a load of the CPU. However, it would have been obvious to a person of ordinary skill in the art, recognizing that both the remaining battery capacity and the CPU load are factors which may be considered as a reason for altering a bus clock frequency to save power, to create a system that can vary the bus clock frequency based upon the CPU load *and* the remaining battery capacity.

Concerning Claim 20, Atkinson further teaches:

each of the plurality of prescribed throttle rates increases as the detected condition decreases within the range (Figure 4, Items 206 and 212; Column 7, Lines 34-38 and 45-50)

Concerning Claim 21, Yeh teaches:

A bus clock controlling method (Column 3, Lines 28-32) in a computer (Figure 1, Item 10; Column 2, Line 62), comprising:

setting a throttle rate of a clock to a predetermined initial value (Figure 2, Item 100; Column 4, Lines 49-53), the clock being used for a data bus (Figure 1, Item 32; Column 3, Lines 2-5) to which both a controlling device (Figure 1, Item 30; Column 2, Line 67) and a peripheral device are connected;

detecting the pressing of a button by a user (Figure 1, Item 78; Column 4, Lines 41-42).

adjusting the set throttle rate according to the user's button press (Figure 2; Item 104; Column 4, Lines 59-61).

Yeh teaches detecting a button press by a user and determination therefrom of a throttle rate instead of by a load on the CPU or a remaining battery capacity.

Weidner teaches:

Detecting a remaining battery capacity (Weidner, Column 5, Lines 39-41).

Adjusting the set throttle rate in reverse proportion to the detected remaining battery capacity (Column 5, Lines 42-45; a decrease in clock rate is equivalent to an increase in throttle rate).

The motivation for combining Yeh with Weidner can be seen above in the Claim 1 rejection.

Atkinson teaches:

detecting a present load of the CPU (Column 5, Lines 5-7).

adjusting the set throttle rate in reverse proportion to the detected present CPU load (Column 5, Lines 10-17).

The motivation for combining Yeh with Atkinson can be seen above in the Claim 5 rejection.

Atkinson and Weidner do not teach of varying a bus clock frequency based upon at least one of the remaining battery capacity *or* load of the CPU. However, it would have been obvious to a person of ordinary skill in the art, recognizing that both the remaining battery capacity and the CPU load are factors which may be considered as a reason for altering a bus clock frequency

to save power, to create a system that can vary the bus clock frequency based upon the CPU load or the remaining battery capacity.

Concerning Claim 22, Yeh teaches:

A computer (Figure 1, Item 10; Column 2, Line 62), comprising:

means for setting a throttle rate of a data bus clock to a predetermined initial value (Figure 2, Item 100; Column 4, Lines 49-53);

means for detecting the pressing of a button by a user (Figure 1, Item 78; Column 4, Lines 41-42).

means for adjusting the set throttle rate according to the user's button press (Figure 2; Item 104; Column 4, Lines 59-61).

Yeh teaches detecting a button press by a user and determination therefrom of a throttle rate instead of by a load on the CPU and/or a remaining battery capacity.

Weidner teaches:

means for detecting at least a remaining battery capacity (Weidner, Column 5, Lines 39-41).

means for adjusting the throttle rate of the data bus clock based on at least the detected remaining battery capacity (Column 5, Lines 42-45; a decrease in clock rate is equivalent to an increase in throttle rate).

The motivation for combining Yeh with Weidner can be seen above in the Claim 1 rejection.

Atkinson teaches:

means for detecting at least a load of the CPU (Column 5, Lines 5-7).

means for adjusting the throttle rate of the data bus clock based on at least the detected load of the CPU (Column 5, Lines 10-17).

The motivation for combining Yeh with Atkinson can be seen above in the Claim 5 rejection.

Atkinson and Weidner do not teach of varying a bus clock frequency based upon at least one of the remaining battery capacity *and* load of the CPU. However, it would have been obvious to a person of ordinary skill in the art, recognizing that both the remaining battery capacity and the CPU load are factors which may be considered as a reason for altering a bus clock frequency to save power, to create a system that can vary the bus clock frequency based upon at least one of the CPU load and the remaining battery capacity.

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh, Weidner and Atkinson and further in view of Young.

Concerning Claim 10, Weidner further teaches:

said second controller determines the throttle rate in reverse proportion to the detected variable (Figure 2, Items 114l and 114h; Column 5, Lines 22-24; the range of values detected can be one of only two values, low and high).

Weidner and Yeh do not teach of using a bridge controller as the first controller.

Young teaches:

said first controller is a bridge controller (Column 1, Lines 20-23).

10. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh, Weidner and Atkinson and further in view of Parrish.

Concerning Claim 12, Atkinson further teaches:

the second controller comprises:

at least one comparator coupled to receive the detected variable from the detector (the variable is used in a comparison, therefore there must be a comparator that receives the detected variable so that the comparison may be performed), configured to compare the detected variable to a plurality of predetermined values, and further configured to output a result of the corresponding plurality of comparisons (Figure 4, Items 206 and 212; Column 7, Lines 34-38 and 45-50).

Weidner teaches:

a host clock throttler configured to output the throttle rate to the first controller (Column 5, Lines 39-45).

Weidner and Atkinson do not teach a host clock throttler that receives the plurality of comparisons and a power mode signal.

Parrish teaches:

a host clock throttler coupled to receive the plurality of comparisons and a power mode signal (Columns 1 and 2, Lines 64-67 and 1, respectively).

Parrish states that "Controller chips that operate at high clock speeds typically consume more power than controller chips running at lower clock speeds" which "may deplete power sources used to power portable computers" (Column 1, Lines 25-31). He states that while power conservation is important, "when power is supplied by an AC source such as the electrical outlet

130, power conservation may not be an important issue, and it may be desirable to operate the graphics adapter 110 at a higher frequency to provide better graphics performance" (Column 2, Lines 38-42). It would have been obvious to a person of ordinary skill in the art to further include a power mode signal that identifies the power source used in a system as described by Parrish with the combination of Yeh, Weidner and Atkinson because it would have afforded it the additional advantage of deciding whether or not power conservation is really necessary before altering the speed of the bus.

Concerning Claim 13, Weidner further teaches:

the at least one comparator comprises a remaining battery capacity comparator, and wherein the detected variable is the remaining battery capacity (Column 5, Lines 42-45; the comparison occurs as the controller selects an output frequency based upon power remaining).

Concerning Claim 14, Atkinson further teaches:

the at least one comparator comprises a CPU load comparator (Column 7, Lines 19-22), and wherein the detected variable is the load of the CPU (Column 7, Line 8).

Concerning Claim 15, Atkinson teaches:

the at least one comparator comprises a CPU load comparator (Column 7, Lines 19-22).

Weidner teaches:

The at least one comparator comprises a remaining battery capacity comparator (Column 5, Lines 42-45).

Atkinson and Weidner do not teach of the at least one comparator comprising a CPU load comparator and a remaining battery capacity comparator. However, it would have been obvious to a person of ordinary skill in the art, recognizing that both the remaining battery capacity and the CPU load are factors which may be considered as a reason for altering a bus clock frequency to save power, to use the at least one comparator to consider *both* the CPU load and the remaining battery capacity when deciding how to adjust the clock speed of the bus.

Allowable Subject Matter

11. Claims 9 and 23-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

12. Applicant's arguments, see Pages 15 and 16, Lines 17-20 and 15, respectively, filed 1/12/2005, with respect to the rejection(s)of claim(s) 1-8 and 10-21 under Yeh have been fully considered and are not persuasive.

Applicant argues, "A system controller 230 of Yeh does not change the frequency of the host clock signal 234 when providing the same for a front bus 232, a memory bus 235 and a video bus 236, but merely passes through the received host clock signal 234 unchanged" (Page 16, Lines 2-5).

However, Yeh discloses the host clock signal provided to the different busses may be altered (Column 6, Lines 19-26). Therefore, the host clock signal is modifiable, not just passed

through. Accordingly, the rejections based entirely or partially upon Yeh are still considered valid.

13. Applicant's arguments, see Page 16, Lines 10-17, filed 1/12/2005, with respect to the rejection(s)of claim(s) 1-3, 8-16 and 19-22 under Weidner have been fully considered and are not persuasive.

Applicant argues, "Weidner discloses a clock generator where a software controller can select output signal frequency based on amount of power, not for example, a throttle rate of a clock for a bus such as between a CPU and a controller" (Page 16, Lines 14-16).

However, the examiner finds the amount of power remaining *is* the throttle rate. While Weidner does not disclose the clock signal being used for a bus, it is argued above that the combination of Weidner and Yeh would have been obvious to a person of ordinary skill in the art to vary the clock frequency of a bus based on power.

14. Applicant's arguments, see Page 17, Lines 13-16, filed 1/12/2005, with respect to the rejection(s)of claim(s) 5-8, 10-16 and 19-22 under Atkinson have been fully considered and are not persuasive.

Applicant argues, "Atkinson appears to disclose adjusting a system clock frequency based on CPU activity such as memory page misses, IO write cycles or other events. Thus, Atkinson does not appear to disclose adjusting a system clock frequency based on CPU load" (Page 17, Lines 13-16).

Examiner finds that a measure of a CPU's load can be measured by the amount of cache read misses. A high cache read miss rate would suggest the CPU has a high load, while a low cache read miss rate (or a high cache read hit rate) would suggest the processor is not heavily burdened. Atkinson suggests reducing clock frequency when the cache read hit rate surpasses a certain threshold. This is indicative of reducing clock frequency when a CPU load is low.

15. Applicant's arguments, see Pages 17, Lines 4-11, filed 1/12/2005, with respect to the rejection(s)of claim(s) 4 and 10 under Young have been fully considered and are not persuasive.

Applicant argues "Young appears to disclose clock controller 21 and variable speed clock supply 41 respectively can control a clock speed of a clock signal provided to devices coupled to a bus such as the PCI bus 7 and the bus 45" (Page 17, Lines 9-11).

The Examiner agrees that Young discloses the clock signal is provided to devices coupled to a bus. However, according to the language used in the claims, Young is understood to be relevant as the clock signal disclosed by Young is "used for the data bus" as set forth in Claim 1 and "provided to the data bus" as set forth in Claim 8.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew A. Henry whose telephone number is (571) 272-3845. The examiner can normally be reached on Monday - Friday (8:00 am -5:00 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MAH

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100